SN74LS160N

■ Product Introduction

The SN74LS160N is a Synchronous Decade Counter (direct clear). that is, the output may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. Low-to-high transitions at the load input of this device should be avoided when the clock is low if the enable inputs are high at or before the transition. The clear function is asynchronous and a low level at the clear input sets all four of the flip-flop outputs. The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional getting. Instrumental in accomplishing this function is two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output.

■ Product Features

- Synchronous preset decimal counter (0-9 count)
- Fully compatible with TTL/DTL input logic level
- Low efficiency asynchronous clear 0 terminal
- Have Complementary output function
- With carry output flag RC, multi chip cascade extension can be realized.
- Package format: DIP16, SOP16

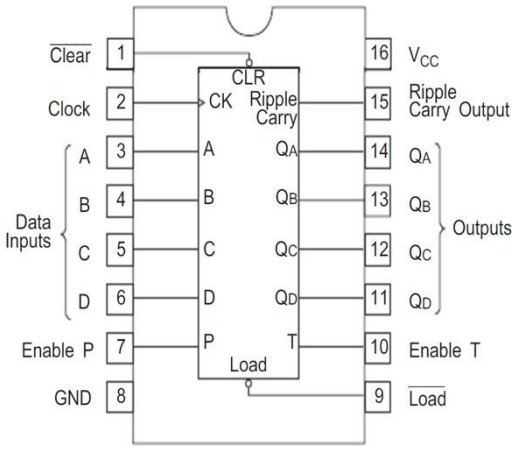
■ Product Applications

- Digital logic driver
- Industrial control application
- Other application areas

■ Package and Pin Assignment

SOP16 or DIP16			
Pin NO	Pin Definition	Pin NO	Pin Definition
1	$\overline{\text{Clear}}$*	16	Supply VCC
2	Clock	15	Ripple Carry Output
3	Input A	14	Output QA
4	Input B	13	Output QB
5	Input C	12	Output QC
6	Input D	11	Output QD
7	Enable P	10	Enable T
8	Supply GND	9	$\overline{\text{Load}}$

Notes: *Asynchronous clear port

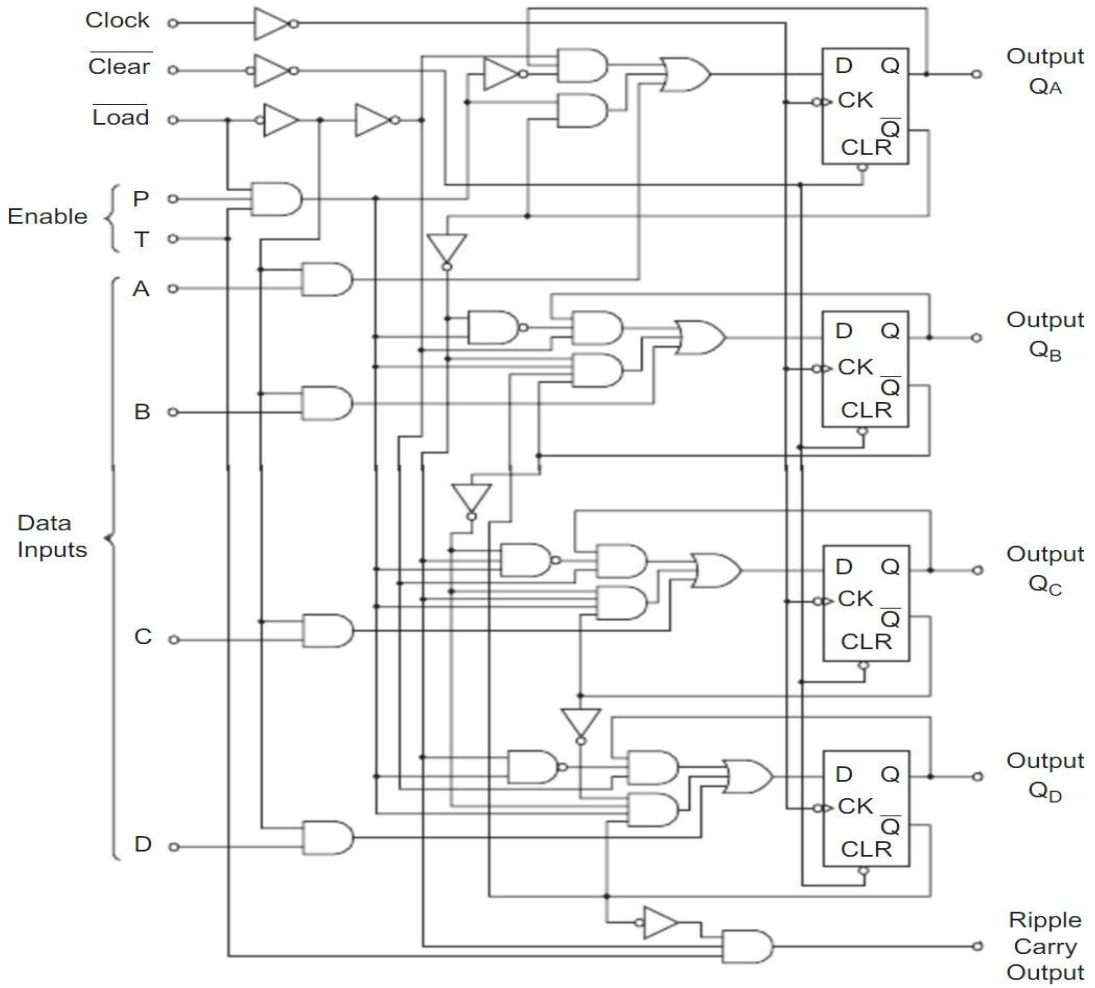


■ Absolute Maximum Ratings

Item	Symbol	Maximum Ratings	Unit
Supply voltage	V_{CC}	7	V
Input voltage	V_I	7	V
Power dissipation	P_D	500	mW
Operating temperature	T_A	0-70	℃
Storage temperature	T_S	-65-150	℃
Welding temperature	T_W	260,10s	℃

Note: the limit parameter is the limit value that cannot be exceeded under any condition. Once this limit is exceeded, it may cause physical damage such as deterioration of the product. At the same time, the chip can not be guaranteed to work properly when it is close to the limit parameters.

■ Block Diagram



■ Function Table

$\overline{Clear}$	$\overline{Load}$	ENT	ENP	Action on the Rising Clock Edge (⌐)
L	X	X	X	RESET (Clear)
H	L	X	X	LOAD ($P_n \rightarrow Q_n$)
H	H	H	H	COUNT (Increment)
H	H	L	X	NO CHANGE (Hold)
H	H	X	L	NO CHANGE (Hold)

H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial

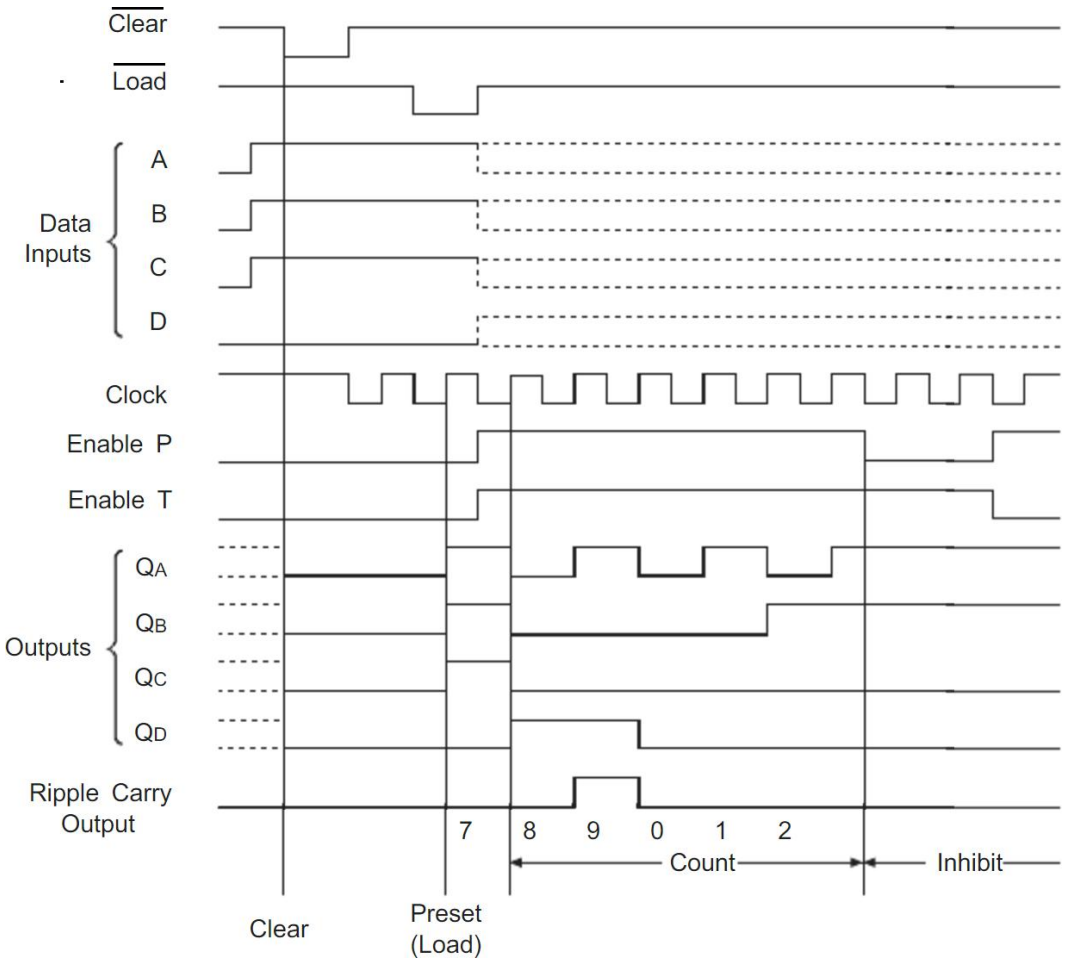
Pn = A B C D Qn= Q_A Q_B Q_C Q_D

Count Enable = $\overline{Load}$ • ENT • ENP

Carry Output = Q_D • $\overline{Q_C}$ • $\overline{Q_B}$ • Q_A • ENT

COUNT=Q_D • $2^{\wedge}3$+Q_C • $2^{\wedge}2$+ Q_B • $2^{\wedge}1$+Q_A • $2^{\wedge}0$

■Typical Clear, Preset, and Inhibit Sequence



■ Recommended Operating Conditions

Item		Symbol	Min	Tpy	Max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output current		I_{OH}	—	—	-400	uA
		I_{OL}	—	—	8	mA
Clock frequency		f_{clock}	0	—	25	MHz
Clock pulse width		t_w	25	—	—	ns
Level pulse width		t_w	15	—	—	ns
Setup time	A、B、C、D	t_{su}	20	—	—	ns
	ENP、ENT	t_{su}	20	—	—	
	$\overline{\text{Load}}$	t_{su}	20	—	—	
Hold time		t_h	3	—	—	
Operating temperature		T_{opr}	0		60	℃

■ Electrical Characteristics

(T_A=25℃, Unless specified)

Item		Symbol	Min	Tpy	Max	Unit	Conditions	
Input voltage		V_{IH}	2	—	—	V		
		V_{IL}	—	—	0.8	V		
Output voltage		V_{OH}	2.7	3.3	—	V	I_{OH}=-400uA	VCC=4.75V,V_{IH}=2V , V_{IL}=0.8V
		V_{OL}	—	0.15	0.4	V	I_{OL}=4mA	
			—	0.25	0.5		I_{OL}=8mA	
Input current	Other	I_{IH}	—	0.1	20	uA	VCC=5.25V, V_I=2.7V	
	$\overline{\text{Clear}}$		—	0.1	20			
	Clock		—	0.1	40			
	$\overline{\text{Load}}$、ENT		—	0.1	40			
	Other	I_{IL}	—	0.25	-0.4	mA	VCC=5.25V, V_I=0.4V	
	$\overline{\text{Clear}}$		—	0.25	-0.4			
	Clock		—	0.22	-0.8			
	$\overline{\text{Load}}$、ENT		—	0.5	-0.8			
	Other	I_I	—	0.1	100	uA	VCC=5.25V, V_I=7V	
	$\overline{\text{Clear}}$		—	0.1	100			
	Clock		—	0.1	100			
	$\overline{\text{Load}}$、ENT		—	0.1	100			
Short-circuit output current *		I_{OS}	-20	-36	-100	mA	VCC=5.25V	
Supply current**		I_{CCH}	—	16	31	mA	VCC=5.25V	
		I_{CCL}	—	17	32		VCC=5.25V	
Input clamp voltage		V_{IK}	—	-1.0	-1.5	V	VCC=4.75V, I_I =–18mA	

Notes: * only one output port is short circuited each time, and the short circuit time is not more than one second.

**I_{CCH} is measured with the load input high, then again with the load input low, with all other inputs high and all outputs open. I_{CCL} is measured with the clock input high, then again with the clock input low, with all other inputs low and all

outputs open.

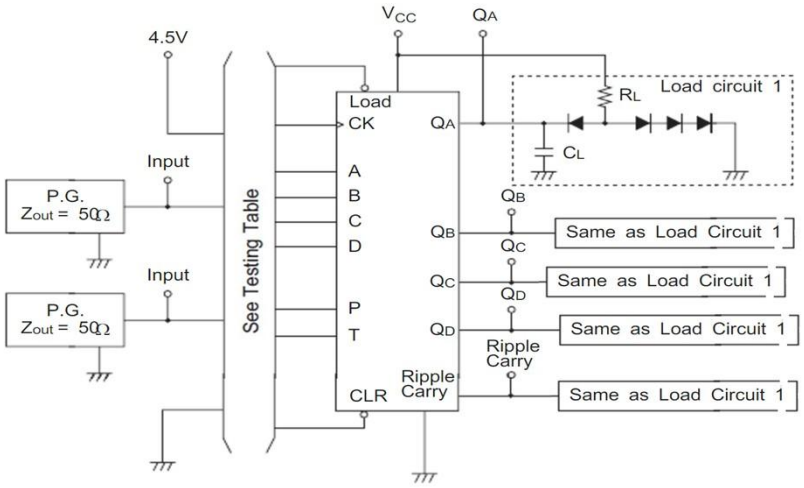
■ Switching Characteristics

(T_A=25℃, Unless specified)

Item	Symbol	Min	Tpy	Max	Unit	Conditions
Maximum clock frequency	fmax	0	20	—	MHz	
Propagation delay time Clock to RC	t_{PLH}	—	50	—	ns	V_{CC}=5V C_L=16pF R_L=2K
	t_{PHL}	—	50	—	ns	
Propagation delay time Clock to Qn	t_{PLH}	—	12	—	ns	
	t_{PHL}	—	20	—	ns	
Propagation delay time ENT to RC	t_{PLH}	—	12	—	ns	
	t_{PHL}	—	20	—	ns	
Propagation delay time $\overline{\text{Clear}}$ to Qn	t_{PHL}	—	20	—	ns	

■ Testing Method

1、Test Circuit

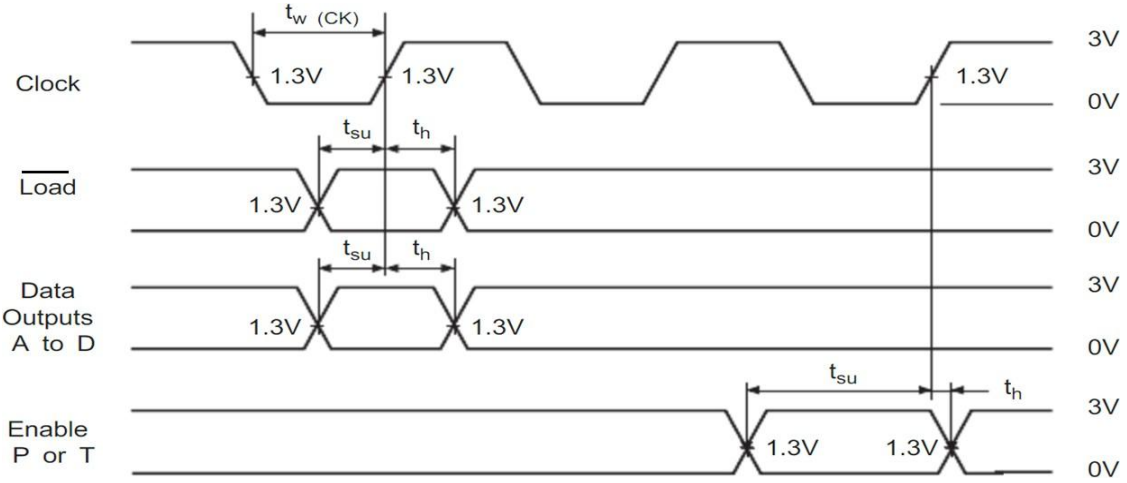


Notes:

1. See Testing Table refers to the corresponding test items in the switch characteristic table.
2. the CL capacitor is an external patch capacitor (0603), which is connected to the output pin and the capacitor is near the chip GND.
3. Input: port input level, f=500kHz, D=50%, tTLH=tTHL= 20ns;
4. .All diodes are 1S2074(H).

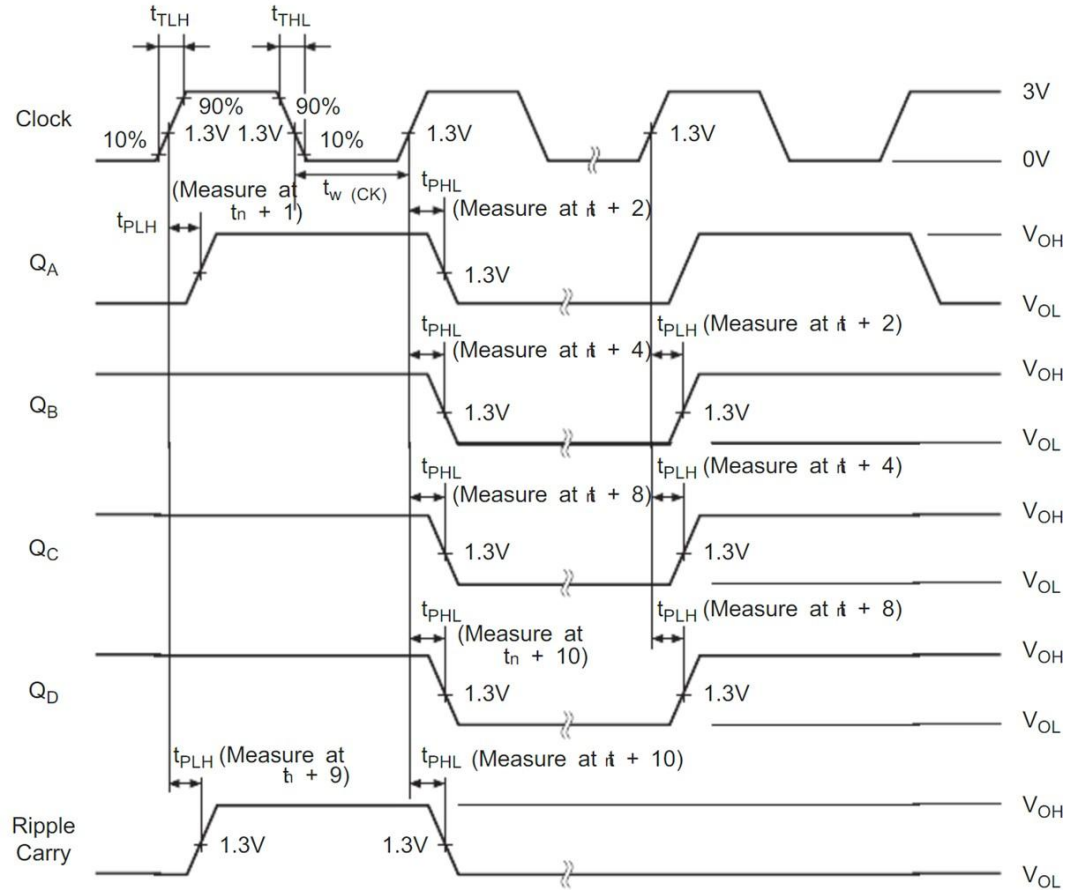
Item	From input to output	Inputs								
		$\overline{\text{Clear}}$	$\overline{\text{Load}}$	Enable		Clock	Data			
				P	T		A	B	C	D
f_{max}		4.5V	4.5V	4.5V	4.5V	IN	GND	GND	GND	GND
t_{PLH} t_{PHL}	CK → Ripply Carry	4.5V	4.5V	4.5V	4.5V	IN	GND	GND	GND	GND
	CK → Q	4.5V	4.5V	4.5V	4.5V	IN	GND	GND	GND	GND
	CK → Q	4.5V	GND	GND	GND	IN	IN	IN	IN	IN
	Enable T → Ripple Carry	4.5V	GND	4.5V	IN	IN	4.5V	GND	GND	4.5V
	CLR → Q	IN	GND	GND	GND	IN	4.5V	4.5V	4.5V	4.5V

2、Waveform 1



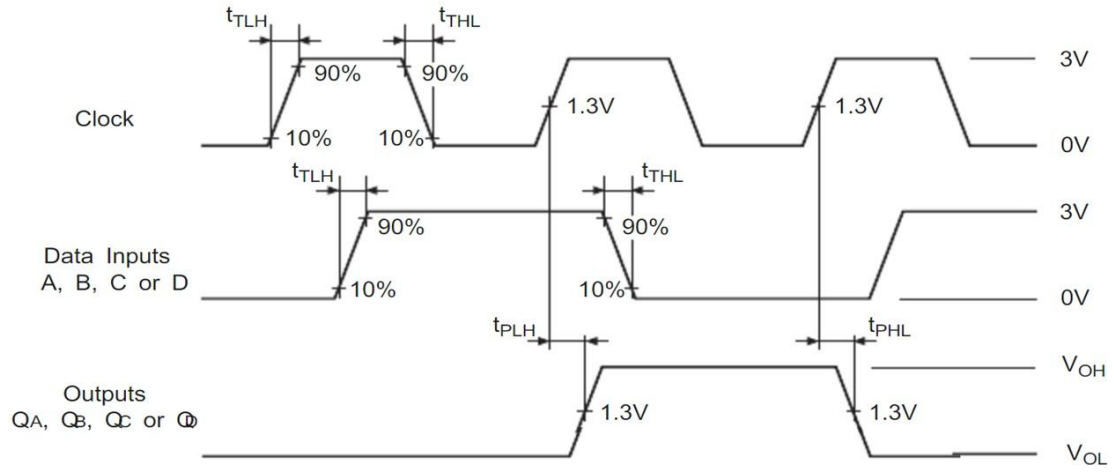
3、Waveform 2

1. f_{max}, t_{PLH}, t_{PHL}, (Clock→Q, Ripple Carry)

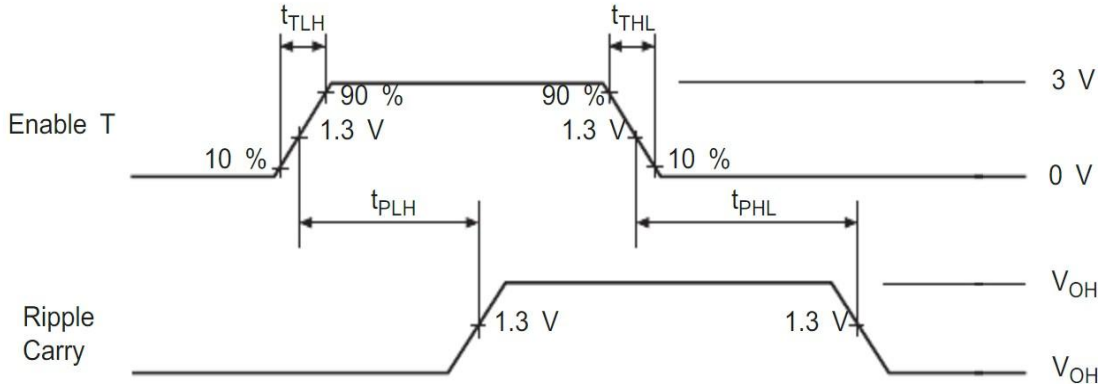


Notes:tn： While all output is low.

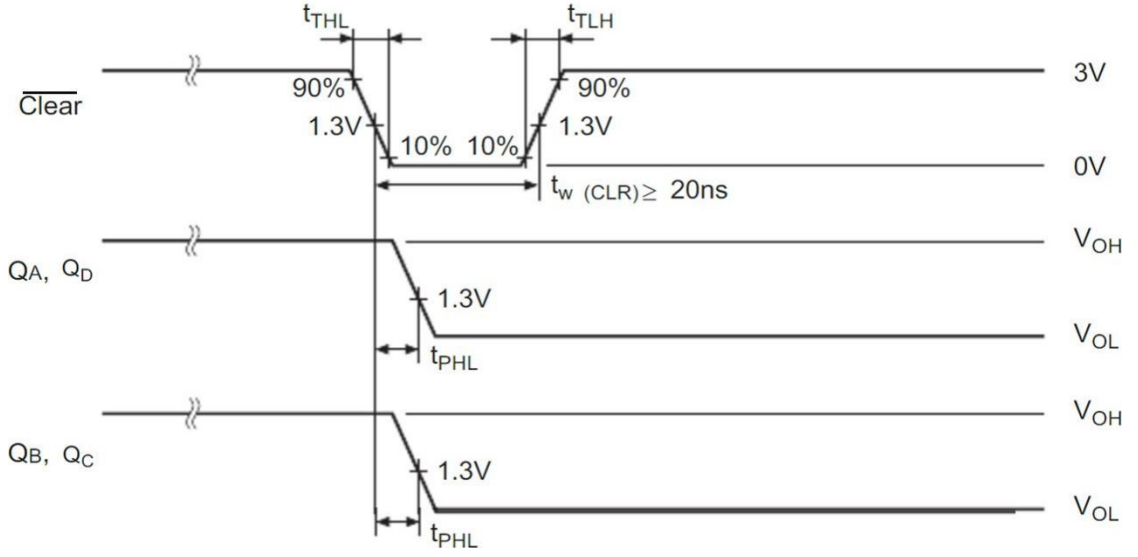
2. t_{PLH}, t_{PHL}, (Clock→Q)



3. t_{PLH}, t_{PHL}, (Enable T→Ripple Carry)



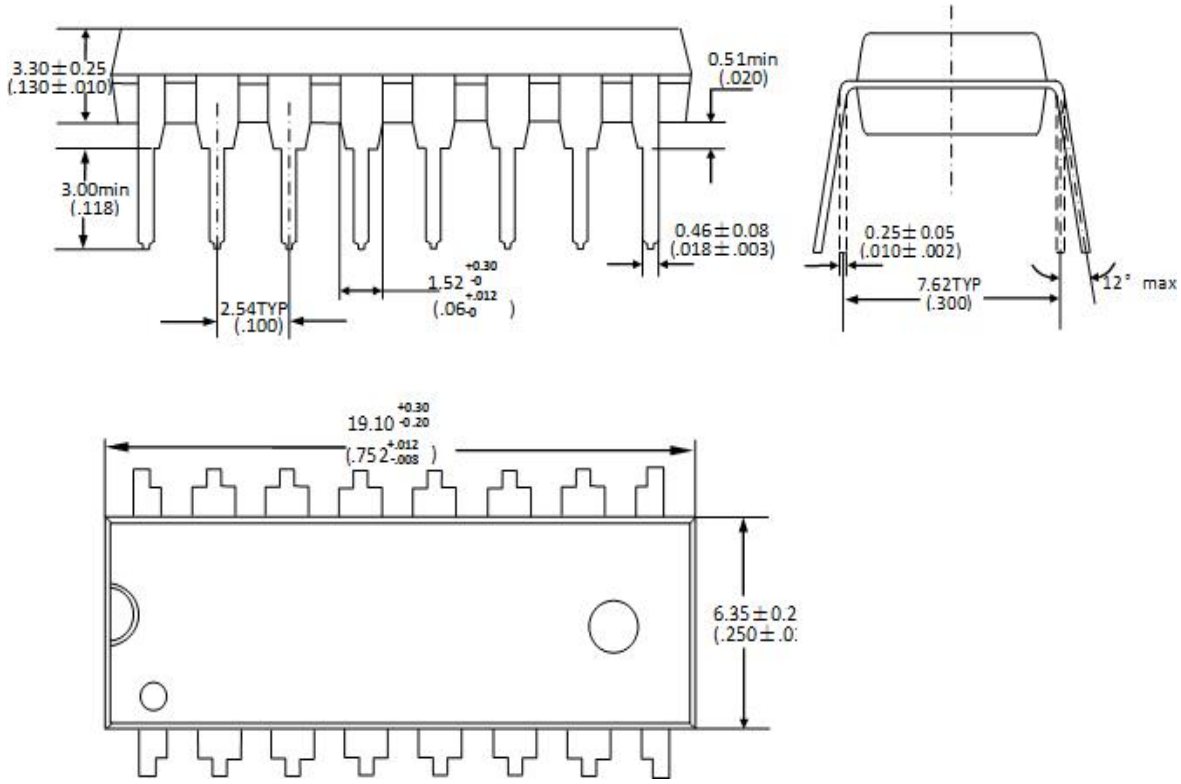
4. t_{PHL}, (Clear→Q)



■ Package Dimensions

Unit : mm /inch

DIP16



SOP16